Team Name: sdmay24-21
Team Members: Yu Wei Tan, Haris Khan, Samuel Heikens, Jonathan Hess
Report Period: Oct 23-Nov 5

Summary of Progress in this Period

Completed a variety of tasks such as the compression Verilog module, adder, and more. Short-listed suitable data converters, updated top level design diagram, defined the scope and design of control module, updated python scripts to use 16bit values, etc.

Pending Issues

SPI module, SRAM research, PCB design & testing research, control module.

Plans for Upcoming Reporting Period

We plan on resolving the aforementioned pending issues.
