Team Name: sdmay24-
Team Members:
Report Period: Sept 25-Oct 8

Summary of Progress in this Period

Finished top level design, started dividing and assigning individual workloads, started looking into specific types of ADC / DAC that are compatible with our design, started working on Verilog HDL code.

Pending Issues

We still need to select analog components that are compatible with our digital design and PCB. In addition, we also need to finish implementing the queue memory module.

Plans for Upcoming Reporting Period

We will resolve the pending issues, and we will also define and meet the specific requirements for our project.