Team Name: sdmay24-21

Team Members: Haris Khan, Yu Wei Tan, Sam Heikens, Jonathan Hess

Report Period: Sept 11-Oct 24

Summary of Progress in this Period

In this period we have decided that we are going to do a digital chip that will modify signals from a guitar pedal using three different effects. We have drawn block diagrams of how this will work and have modeled the different inputs and outputs that are needed for this. We have also specified how many data converters will be needed for our PCB.

Pending Issues

We need to finalize the installation of docker on some member's devices. We also need to check in with our professor with our project plan. We also need to start our digital design in verilog as soon as possible.

Plans for Upcoming Reporting Period

These tasks are in the next reporting period.

- i. Define the scope & specifications of our project
 - a. Brainstorm a specific application for our project
 - b. Compile a list of functions that may be relevant to our project
 - c. Need a project that can be finished within time frame necessary and also challenging enough
- ii. Install and familiarize ourselves with the workspace on Docker
 - a. Install digital tools that we will use to design our project
 - b. Familiarize ourselves with how to do basic design in the tool and how it can be integrated with EFabless
 - c. This task is necessary so we can design our chip with these tools
- iii. Design a top level diagram for the user area
 - a.
 - b. This task in necessary for us to decompose our project into blocks
- iv. Meticulously design each module in Verilog
 - a. Each module will be given a set of inputs and output and requirements to be met
 - b. Each module will be designed
 - c. Each module will be verified for proper functionality

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- d. This task is necessary so that we can assemble all of our modules
- e. During this time off chip data converters will be selected