EE/CprE/SE 491 WEEKLY REPORT 4

SDMAY24-21

Digital ASIC Fabrication

2/23/2024 - 3/30/2024

Client & Advisor: Dr. Henry Duwe

Team Members/Role:

Yu Wei Tan

Samuel Heikens

Haris Khan

Jonathan Hess

- **Weekly Summary**

  Our team started working on our assigned parts, and have made progress. Our project is projected to be completed on time.

- **Past week accomplishments**

  • Jonathan: Started working on the design and implementation of the memory controller and testbenches.

  • Haris: During this week Haris was working on the top level design and integration

  • Yu Wei: Yu Wei finished a working prototype of the PCB. After receiving feedback from Dr. Duwe, he is currently working on the final design of the PCB.

  • Samuel: During this week, Samuel has finished the SRAM module with the help of Jonathan and Haris. He has also setup on a linux environment to run Hardenign, rtl simulations, and GL simulations locally. Currently he is working on the hardening process.

- **Pending issues**

  • Jonathan: Finish memory controller and add testbenches to verify functionality.

  • Haris: Haris need to finish the memory as well as test it, SPI also needs to have integration testing

  • Yu Wei: Yu Wei is working to include an audio jack module on the PCB so the ASIC can receive and output audio signals.

  • Samuel: There are errors being generated by the hardening process that need to be resolved for the hardening process to run.

- **Individual contributions**

NAME	Individual Contributions *(Quick list of contributions. This should be short.)*	Hours this week	HOURS cumulative
Jonathan	Memory Controller Module and Testbenches	6	16
Haris	Worked on top level design, integration of components	15	
Yu Wei	PCB design (with off-chip components)	18	38
Samuel	Finished SRAM Setup up local run of Openlane Met with other team to better understand hardening and precheck Worked to resolve errors in hardengin process	20	40

o **Plans for the upcoming week**

- Jonathan: Finish memory controller and add testing to verify design.
- Haris: To finish and test the memory module as well as learning more about verilator
- Yu Wei: Yu Wei plans to finish the final design for the PCB, and create a test plan to ensure we can debug the circuit.
- Samuel: Samuel will continue to resolve errors in the hardening process.

o **Summary of weekly advisor meeting**
Notes:
- Testing with off chip components
- Add audio jack on board
- We need test plan