***EE/CprE/SE 491 WEEKLY REPORT 3***

***2/8/20 – 2/22/2024***

***Group number: sdmay24-21***

***Project title: Digital ASIC Fabrication***

***Client &/Advisor: Dr. Henry Duwe***

***Team Members/Role: Yu Wei Tan, Samuel Heikens, Haris Khan, Jonathan Hess***

- **Weekly Summary**

  Our team is very split up right now due to the different tasks currently in progress. In general we learned more about our Design Tools, and we worked on our parts of the design for the project. Our progress has been slower than expected.

- **Past week accomplishments**

  • Jonathan: Laid out timing diagram for memory controller and data throughput of SPI connections.

  • Haris: Haris was still working on the Memory control module as well as placing example designs into Verilator to get used to the process

  • Yu Wei: Yu Wei continued learning about KiCad PCB design by starting to experiment with sample PCB layouts. Yu Wei also started looking up PCB designs that were made by previous Efabless teams to have a better understanding on what the final design should look like.

  • Samuel: Samuel attempted to run Openlane through GitHub. The process was difficult so Samuel contacted Gregory and Jake from a previous team. They recommended that Openlane be run locally instead of through GitHub. With help from Jonathan, Samuel started setting up the local environment. Samuel also continued to learn more about the SRAM.

- **Pending issues**

  • Jonathan: Creation of the first testbench level (no control/SPI modules) and finishing memory controller module.

  • Haris: Need to work on the memory controller and top Level integration

  • Yu Wei: Yu Wei still has to start working on prototype PCB designs to ensure the final design is suitable for our ASIC.

  • Samuel: The local Openlane environment still needs to be set up.

- **Individual contributions**

| **NAME** | **Individual Contributions** *(Quick list of contributions. This should be short.)* | **Hours this week** | **HOURS cumulative** |
|---|---|---|---|
| Jonathan | Memory Controller Module and Testbenches | 4 | 16 |
| Haris | Working on memory controller as well as utilizing Verilator | 6 | 20 |
| Yu Wei | Continued with the PCB design research | 6 | 20 |
| Samuel | Attempted to run Openlane, connected previous team, started local Openlane setup | 6 | 20 |

- **Plans for the upcoming week**

  • Jonathan: Finish testing memory controller design and use Verilator to test top level design.

  • Haris: Haris Plans to test the memory controller and top level design

  • Yu Wei: Yu Wei Plans to start working on the final design

  • Samuel: This week Samuel plans to finish setting up the local Openlane environment. Samuel also needs to get working on the SRAM instantiation. Samuel also wants to run the SRAM through Openlane to see the hardened SRAM as well as test the local Openlane to ensure that it is running correctly.