EE/CprE/SE 491 WEEKLY REPORT 2

1/25/20 – 2/8/2024

Group number: sdmay24-21

Project title: Digital ASIC Fabrication

Client &/Advisor: Dr. Henry Duwe

Team Members/Role: Yu Wei Tan, Samuel Heikens, Haris Khan, Jonathan Hess

- **Weekly Summary**

  Our team is very split up right now due to the different tasks currently in progress. In general we learned more about our Design Tools, and we worked on our parts of the design for the project. Our progress has been slower than expected.

- **Past week accomplishments**

  • Jonathan: Started working on the design and implementation of the memory controller and testbenches.

  • Haris: During this week Haris was working on the testing of the SPI module, As well as making progress on the Memory module in parallel.

  • Yu Wei: Yu Wei started familiarizing himself with KiCAD's (PCB design tool) interface, and started researching Efabless provided resources that would aid in the design of a PCB.

  • Samuel: During this week, Samuel reached out to members from a previous team to get resources on instantiating SRAM cells. Samuel got a couple of resources from their project and looked through them. Samuel also tried to increase his understanding of what SRAM is and what needs to be done.

- **Pending issues**

  • Jonathan: Finish memory controller and add testbenches to verify functionality.

  • Haris: Haris need to finish the memory as well as test it, SPI also needs to have integration testing

  • Yu Wei: Yu Wei is still a novice at PCB design, and still needs more experience working with KiCAD. Yu Wei also needs to compile a bill of materials.

  • Samuel: After meeting with Jonathan, Samuel had a greater understanding of what Samuel is doing.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Jonathan	Memory Controller Module and Testbenches	5	12
Haris	Worked on SPI and Memory	6	14
Yu Wei	Learn about PCB design	6	14
Samuel	Get information from periods team/learn about SRAM/Met with Jonathan	6	14

- **Plans for the upcoming week**

  • Jonathan: Finish memory controller and add testing to verify design.

  • Haris: To finish and test the memory module as well as learning more about verilator

  • Yu Wei: Yu Wei plans to continue learning PCB design, creating sample schematics before designing a PCB for the project.

  • Samuel: Samuel should make a Verilog file and call the SRAM instance 100 times to provide adequate memory for our system.

- **Summary of weekly advisor meeting**

In our meeting this week, we clarified the responsibilities and roles of our team members.
Goals:

1. Simulations + testbenches:

- Test 1: No SPI / Control
- Test 2: Control
- Test 3: SPI + Control

2. PCB design:

- Find + modify the template
- Specify bill of materials + footprints
- Decide soldering responsibilities

3. ASIC design:

- SRAM + Memory Control
- SPI
- Control code

- Adder

Design tools responsibilities

- Verilator: Jonathan
- OpenLane: Sam
- Verilator: Haris
- KiCad: PCB